Resonant Tunnelling Hot Electron Transistors: Present Status and Future Prospects

N. Yokoyama, K. Imamura, M. Takatsu, T. Mori, T. Adachihara, Y. Sugiyama, Y. Sakuma, A. Tackeuchi and S. Muto

Email alerting service	Receive free email alerts when new articles cite this article - sign up in the box at the top right-hand corner of the article or click **here**

Resonant tunnelling hot electron transistors: present status and future prospects

By N. Yokoyama[1], K. Imamura[2], M. Takatsu[1], T. Mori[1],
T. Adachihara[1], Y. Sugiyama[1], Y. Sakuma[1], A. Tackeuchi[1] and
S. Muto[3]

[1] Fujitsu Limited, Fujitsu Laboratories Ltd, 10-1 Morinosato-Wakamiya,
Atsugi 243-01, Japan
[2] Shiga International Patent Office, 3-23-3 Takadano-Baba, Shinjyuku 169, Japan
[3] Hokkaido University, North 13 West 8, Sapporo 060, Japan

We proposed and demonstrated a resonant-tunnelling hot electron transistor (RHET) in 1985, and developed a multi-emitter RHET in 1993, enabling us to make an SRAM cell and multi-input logic gates using a single transistor. Through the development of these quantum tunnelling transistors, we have created the technology needed to fabricate precisely controlled quantum well structures, and have mostly understood the physics behind quantum well structures. Although this technology has been successfully used to develop heterostructure transistors and quantum well laser diodes, RHETs cannot yet be used in practical applications.

One reason is that the RHET should be cooled down to about 77 K and its functionality is insufficient to replace conventional semiconductor devices. To make these RHETs practical for future use in cryoelectronic systems, integration with complementary-HEMT logic circuits or developement of new architecture circuits will be essential.

There are also other important areas of research for us. One is to develop room temperature quantum functional bipolar transistors. Another is to develop quantum box devices based on the RHET technology, searching ultrasmall limit of electron devices. These research will be also useful in the development of photonic devices, such as quantum dot lasers and new photonic memory devices.

---

1. Introduction

Recent research into semiconductor device technology seems to be aimed at reducing costs and decreasing power dissipation of CMOS circuits, rather than developing new and advanced semiconductor devices. The need to reduce the size of devices will continue, even into the next century. When devices enter the nanometre scale, quantum mechanical effects play an important role in device's function. Therefore, it is important to continue basic research in this area to cultivate these new 'nanoelectronic' devices.

Recent quantum effect nanometre-scale devices can be divided into three categories. (1) Quantum wave devices, which use the electron-wave transport and control the phase of the electron wave. (2) Quantum functional devices, which use quantum effects, such as size and tunnelling effects in ultrafine structures. Single electron de-
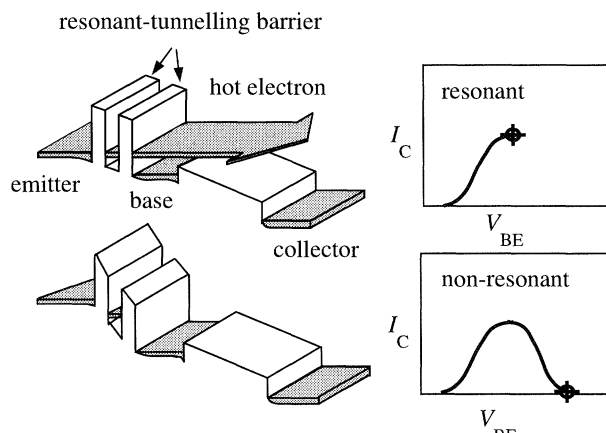
Figure 1. Operation of RHET.

vices could be included in this device category. (3) Atomic or molecular devices, which use the motion of atoms or molecules.

In 1985 we proposed and demonstrated a resonant-tunnelling hot electron transistor, or RHET (Yokoyama *et al.* 1985), which exhibits a negative transconductance. Using this RHET, we decreased the number of transistors needed in full adders to about one quarter that of conventional bipolar circuits. The RHET could be called the first quantum functional device. This paper describes current status and future prospects of RHET technologies and outlines future research directions to develop quantum-tunnelling electronic and photonic devices.

2. RHET technology

Figure 1 shows the operation of an RHET, which uses a resonant-tunnelling barrier between the emitter and the base. When a particular voltage is applied to the base, electrons are injected from the emitter to the base by resonant-tunnelling effects. Electrons that travel through the base region, reach the collector and contribute to the collector current. When the base voltage increases further, the resonant-tunnelling effect decreases, as does the collector current. Hence, the RHET exhibits a negative transconductance. Since it uses hot electron transport, the RHET is expected to be extremely fast.

Using RHETs, we decreased the number of transistors needed in logic circuits. In 1989 we developed a RHET full adder consisting of two exclusive NOR gates and a three input majority logic gate. The number of transistors used in this circuit is about a quarter of that used in conventional bipolar circuits. However, the many resistors needed in these RHET circuits limited the circuits' speed, power performance, and scale of integration.

Our multi-emitter RHET overcomes these problems (Takatsu *et al.* 1994). The top two diagrams in figure 2 show cross-sections of conventional and double-emitter RHETs. The double-emitter RHET is essentially the same as the conventional RHET, but it has two separate emitters and no base electrodes. With the conventional RHET, electrons in the emitter are injected into the base layer under normal bias conditions. Electrons, scattered in the base region, drain to the base electrode.

The double-emitter RHET turns on when the voltage difference between the emit-
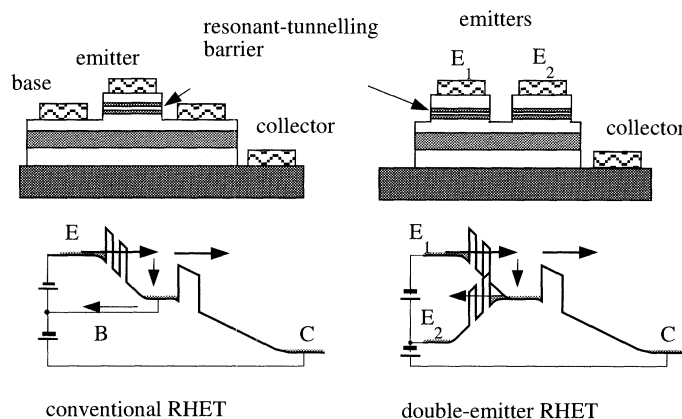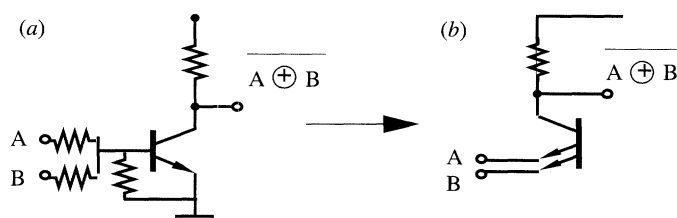
Figure 2. RHET structures and band diagrams.

Figure 3. Exclusive-NOR gates. (*a*) Conventional RHET. (*b*) Double-emitter RHET.

ters exceeds a certain threshold that is the sum of the emitter barrier's forward and reverse turn-on voltages. The low potential emitter works as an injector of electrons and the high potential emitter works as a sink for scattered electrons, like the base contact of conventional RHETs. Thus the emitter plays a different role depending on its potential.

When the two emitters have the same potential, either both high or both low, the RHET is off.

Figure 3 compares exclusive-NOR circuits that are fabricated both with conventional RHETs and with the new double-emitter RHET. The conventional RHET exclusive-NOR gate needed three resistors for an input-voltage adder. In the new circuit, we can feed the input signals directly to the emitters and take the collector voltage as the output. The input signals' logic swing crosses the emitter's threshold.

The output is high when the multi-emitter RHET is off. This condition is satisfied only when both inputs are in the same logic state. When low-level and high-level inputs occur together, the potential difference between the two electrodes exceeds the threshold, and the transistor turns on. The output then goes low. This indicates that the circuit acts as an exclusive-NOR gate. Using a multi-emitter RHET, we can omit resistors from exclusive-NOR gates.

We then examined a triple-emitter RHET structure. We fed three input signals to the three emitters and took the collector voltage as the output, as shown on the left in figure 4. The output is high when the triple-emitter RHET is off. Again, this condition is satisfied only when all the inputs are in the same logic state. The circuit's logic is described as $\mathrm{ABC} + \overline{\mathrm{ABC}}$, and it functions as a three input AND/NOR gate. Since the subtraction of input voltages is done in the transistor, no external elements except a load resistor are needed. If we build 3-input AND/NOR gates using bipolar
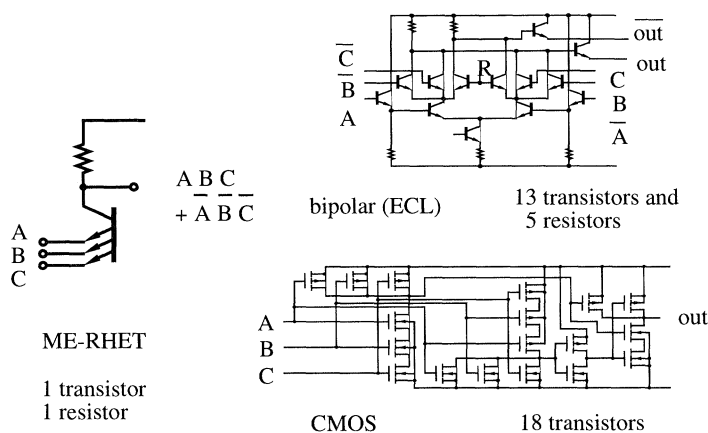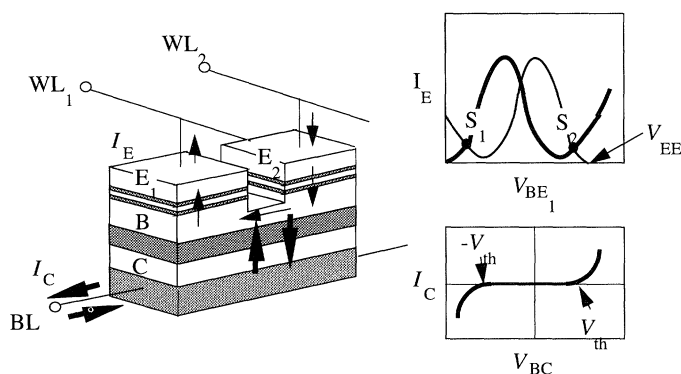
Figure 4. Three input AND/NOR gates.

Figure 5. Double-emitter RHET SRAM cell.

or CMOS circuits, we need 18 elements including both transistors and resistors. The AND/NOR gate using a multi-emitter RHET consists of only two elements. We can increase the number of emitters to four or more to build various multi-input logic circuits with fewer transistors.

We measured the propagation delay time of this NOR gate using a 25-stage ring oscillator fabricated using $16\,\mu\text{m}^2$ emitter RHETs. The propagation delay was estimated to be 130 ps at 77 K with a supply voltage of 2.5 V. The emitter current density was as low as $6000\,\text{A cm}^{-2}$. By scaling down the device size to $1\,\mu\text{m}^2$ with a self-aligned structure, the delay will be decreased to around 10 ps. The reduction in the number of components is expected to result in the reduction of wire delay and power consumption.

3. RHET memory devices

To build a memory cell, we connected word lines WL_1 and WL_2 to emitters E_1 and E_2, as shown in figure 5 (Mori *et al.* 1993). We also connected the bit line BL to the subcollector. Each emitter has an n-shaped negative differential resistance region, giving two stable states, S_1 and S_2, when a suitable voltage is applied between WL_1 and WL_2. The electron potential of base region B is higher for S_1 than for S_2.

The main feature of this device application is the read and write operations, which
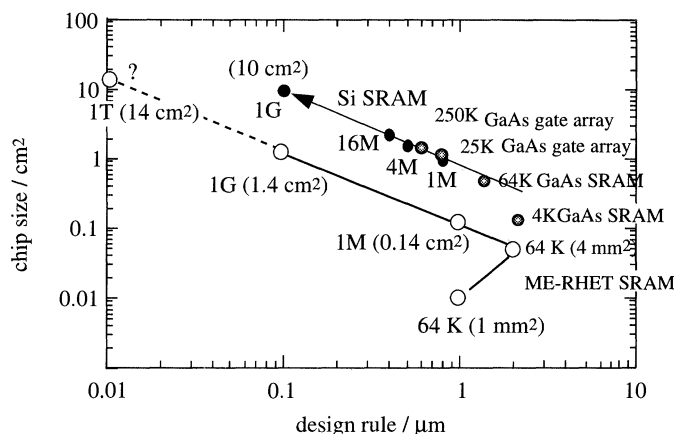
Figure 6. Chip sizes plotted as functions of design rule.

are done using its collector barrier current–voltage characteristics. No current flows when the base-collector voltage is low. The current increases and decreases quickly with collector-base voltages above and below the bias thresholds.

By fabricating a cell array with a resonant-tunnelling emitter of 16 μm^2, we confirmed that the proposed cell can be used as an SRAM cell. It should be noted that while conventional MOSFET and GaAs MESFET uses six transistors per SRAM cell, our new cell uses only one transistor. By combining the SRAM cell array and logic circuits using multi-emitter RHETs, we can build an SRAM chip having the chip 1/7 the size of conventional GaAs and CMOS SRAM chips.

We are now redesigning the RHET structure to decrease standby power dissipation of memory cell, maintain the high speed operation of RHET logic circuits.

4. Manufacturing RHET circuits

Fujitsu opened a plant to produce GaAs digital ICs in 1991 at a cost of about $250 million. The plant has 3000 m^2 of Class 10 clean rooms, and computer-controlled equipment for 4-inch GaAs wafers is fully automated, operating 24 hours a day. In this plant, 25 K GaAs MESFET gate arrays with a gate length of 0.8 μm, and a 10.7 mm by 10.7 mm chip have been produced for supercomputer applications. Fujitsu announced the VPP500-series supercomputer system which uses 45 GaAs chips per processor element and operates at 1.6 GFLOPs. The system uses a vector parallel architecture for the vector unit and a long instruction word type RISC architecture for the scalar unit, demonstrating 355 GFLOPS using 222 processor elements. This indicates that the system uses about 10 000 GaAs chips, counting the total gate number of 250 million. At present, 250 K GaAs gate arrays can be fabricated at the plant and this is one order higher integration level than that used in supercomputers. The chip size is 1.2×1.2 cm^2, the largest chip size being available in our plant where 4 inch GaAs wafer line is adopted.

Figure 6 plots the chip sizes of Si SRAM devices, GaAs SRAM devices and GaAs gate arrays, together with the estimated sizes of our ME-RHET SRAM devices as functions of the design rule. Spherical plots show 250 K and 25 K GaAs gate arrays, and 64 K and 4 K GaAs SRAM. These are technically manufacturable in the plant. Although the gate arrays are commercially available, the SRAM devices are not. This

is because the price will be an order of magnitude higher than Si SRAM devices using the same integration level.

Open circles indicate the estimated size of our ME-RHET SRAM chips. It should be noted here that the size of 1 Gb SRAM chips is estimated to be $1.4\,\mathrm{cm}^2$, the same as that of 250 K GaAs gate array, now commercially available. On the other hand, the size of 1Gb Si SRAM chips is estimated to be up to $10\,\mathrm{cm}^2$, requiring the establishment of new 10 inch or 12 inch wafer plant. From this point of view, 1 Gb ME-RHET SRAM could be price-competitive with 1 Gb Si SRAM chip in future, assuming that the production yield of our new SRAM is comparable to or higher than that of conventional SRAM because of the reduced number of elements and chip size. To get a reasonable production yield, the development of an atomically-controlled, high-quality epitaxial growth technique for mass production is essential.

Even though the prices are becoming comparable, ME-RHET SRAM will not really be able to compete with Si RAMs since we have to cool it to 77 K.

An application of these quantum functional devices, therefore, will be limited to cryoelectronic systems, such as high-end GaAs supercomputer systems, asynchronous transfer mode (ATM) data switches with very high throughputs of over $1\,\mathrm{Tb\,s}^{-1}$, and for very high performance image processing. In these systems, quantum functional devices will be integrated with complementary-HEMT logic circuits on a chip or board. High-temperature superconducting technology could also be used for inter-connections between chips or boards. Otherwise, quantum functional devices will be used in new architecture circuits.

5. Future research

One direction is to develop quantum functional transistors operating at room temperature. Another aim is to search for quantum box devices for developing electronic and/or photonic devices, impossible using Si technology. In this paper, we describe the room temperature quantum functional bipolar transistors and quantum box fabrication technology that we developed recently, and discuss their possible device applications.

(a) Room temperature quantum functional bipolar transistors

The quantum functional bipolar transistors we developed for room temperature operation have two separate emitters and no base electrodes (Imamura *et al.* 1994). Figure 7 shows their operation. The key to this device is the use of a heavily doped base and emitters, which allow band-to-band tunnelling in reversed bias conditions.

When emitters E_1 and E_2 are in the same logic state, either low or high, there is no collector current since the base is open. When we apply a positive bias on emitter 2 with respect to emitter 1, the base potential is pulled down due to the band-to-band tunnelling in emitter 2. Electrons are then injected from the forward biased emitter 1 to the base region, turning the transistor on. Since emitters 1 and 2 are symmetric, the transistor also goes on when positive bias is applied to emitter 1 with respect to emitter 2.

The device is thus similar to the double emitter RHET and is switched on or off depending on the voltage difference between the two emitters. Therefore, we can increase the number of emitters to three or more. The important difference between them is that the multi-emitter HBTs operate at room temperature but do not have a negative conductance region. If we integrate a resonant tunnelling
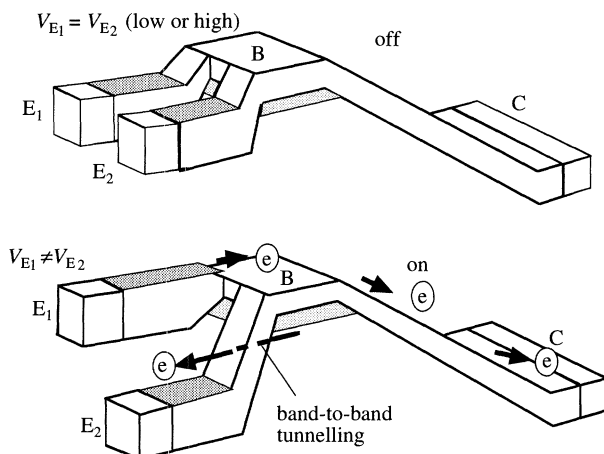
$V_{E_1} = V_{E_2}$ (low or high)

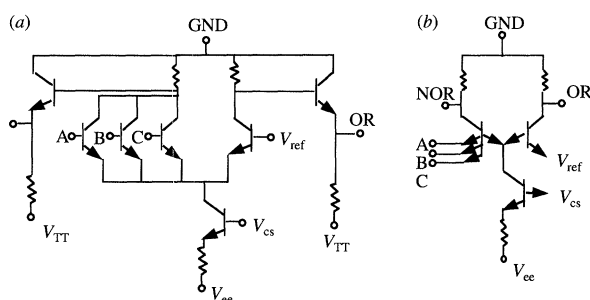Figure 7. Operation of quantum functional bipolar transistor.

Figure 8. Three-input ECL logic gates designed for conventional and multi-emitter HBTs. (*a*) Conventional ECL. (*b*) ECL using ME-HBTs.

barrier or interband tunnelling barrier with a series of emitters, the device can have a negative conductance region, enabling us to build a memory cell.

Figure 8 shows three input ECL logic gates designed for multi-emitter HBTs, and compares them with those for conventional HBTs. The new ECL gate uses a quadruple-emitter HBT. One of the four emitters is fixed low by connecting to the current source, and therefore the quadruple-emitter HBT is off when inputs A, B, and C are all low. For other combinations, the transistor goes on. So, the circuit acts as a three- input NOR/OR gate. It should be noted here that the new circuit does not need an emitter follower for each output because the reverse biased emitter, acting as a current sink, acts as a level shifter in itself.

The fabrication process for the multi-emitter HBT is simpler than that for a conventional HBT. This is because the multi-emitter HBT does not need the process for the base contact formation process. Thus this device could potentially be used in existing HBT digital circuits.

(*b*) *Quantum box structures*

Figure 9 shows the history of the development of GaAs electron devices. As with Si devices, there is a trend of scaling the size of GaAs MESFETs or HEMTs devices. The other technological trend in GaAs devices is that new physical phenomena occur with reducing the size, enabling us to develop devices using new operating principles.
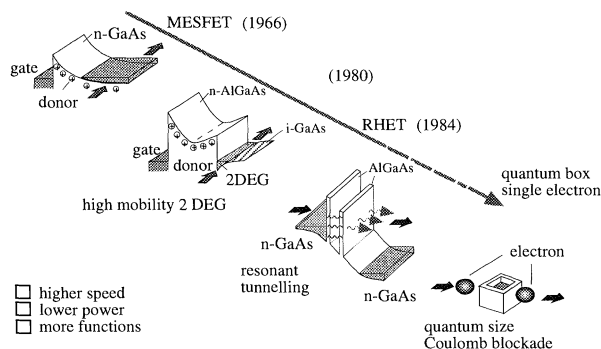
Figure 9. History of the development of GaAs electronic devices.
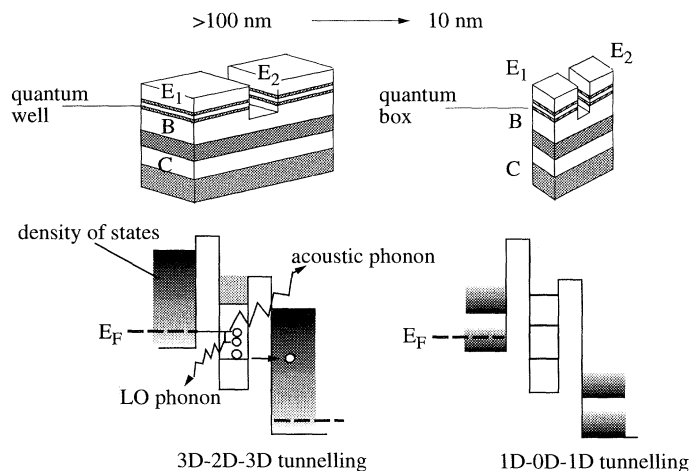

Figure 10. Simplified band diagrams for quantum-well and quantum-box emitters.

This comes from the advantage of GaAs devices over Si devices in that we can design and make artificial electron potential in the direction of crystal growth by combining various kinds of compound semiconductor materials. Following the development of GaAs MESFETs, HEMTs with precisely controlled heterojunctions, and RHETs with atomically controlled quantum well structures have been developed.

The next trend may be to develop quantum box devices where electron states are quantized in all three dimensions.

When the size of multiple-emitter RHETs reaches the 10 nm range, the quantum-well emitter becomes a quantum box emitter. The electron transport is thus changed due to lateral confinement. The bottom two figures in figure 10 show simplified band diagrams for both emitters in non-resonant states. The black-shaded areas show the density of states for each layer, and the dashed lines denote the Fermi level. The density of states is proportional to the square root of the energy for three-dimensional emitter and base layers, independent of the energy for the two-dimensional layer, and inversely proportional to the square root of energy for the one-dimensional layer. It then takes a delta function distribution for the zero-dimensional layer.

For quantum well emitters, shown on the left of figure 10, electrons can be injected into the base layer through the two-dimensional quantum well, helped by scattering events with LO and/or acoustic phonons.

1. Use of GaAs (111)B substrates

2. Anisotropic etching
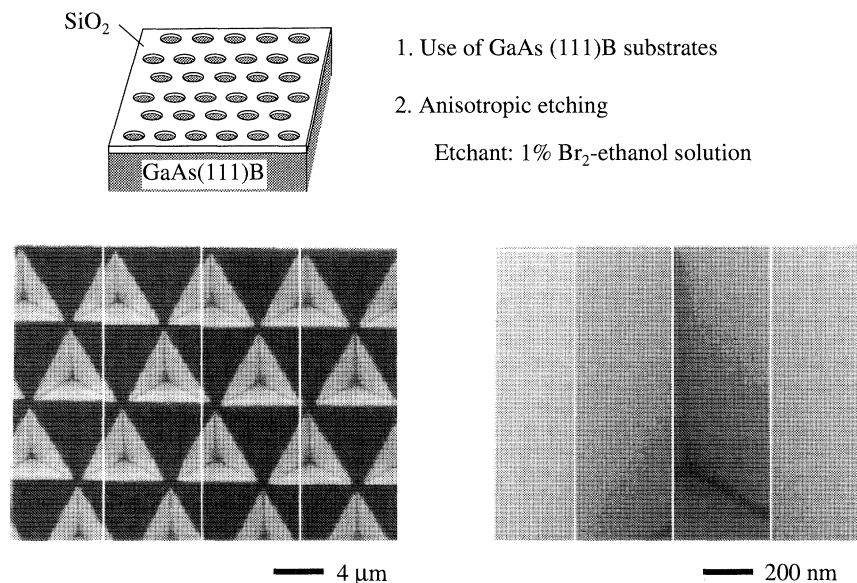
   Etchant: 1% Br_2-ethanol solution

Figure 11. Inverted tetrahedral-shaped recesses (TSR) using GaAs (111)B substrates.

For quantum box emitters, shown on the right, quantized energy levels in the quantum box separate completely, and the separation energy could be larger than the longitudinal optical phonon energy. In such a regime, we expect that electrons cannot be injected due to reduced scattering events in quantum box, thus decreasing the valley current.

Clearly, we must develop a new nanostructure process technology to make ideal quantum box structures, and then we must further investigate the physics of quantum boxes, particularly the tunnelling mechanism and the interactions between electrons and phonons in such nanometre structures.

We have recently proposed the use of (111)B substrates to make quantum boxes (Sakuma *et al.* 1994). If we use (111)B substrates and anisotropic etching using a 1% bromine ethanol solution, we can make inverted tetrahedral-shaped recesses (TSR) having three kinds of (111)A facets, converging to a very sharp bottom. Figure 11 shows an SEM picture of the etched surface and a magnified view of the bottom of the TSR. We found that TSR arrays are regularly formed as expected. The (111)A facets are very smooth and the bottom of the TSR is very acute. We attempted to make quantum box structures by growing an AlAs/GaAs heterostructure at the bottom of the TSR. A 15 nm thick and 30 nm wide box-like GaAs structure was obtained. The advantage of this method is that we can position these artificial boxes using a mask-window. The sizes of the boxes are automatically reduced to less than the lithographic limit. Identical boxes can be formed based on the uniform shape of the TSRs.

More recently, we formed a novel InGaAs/GaAs quantum box structure in the TSR. Smooth sidewalls were successfully grown even under the mask. Using TEM observations, we confirmed that no dislocation was observed in the bottom and in other areas. Figure 12 shows the photoluminescence (PL) of the pseudomorphic heterostructure with a thin InGaAs layer of 2.5 nm and cathode luminescence image taken at 1.45 eV and 1.48 eV, where the PL spectrum shows two clear peaks.

N. Yokoyama and others

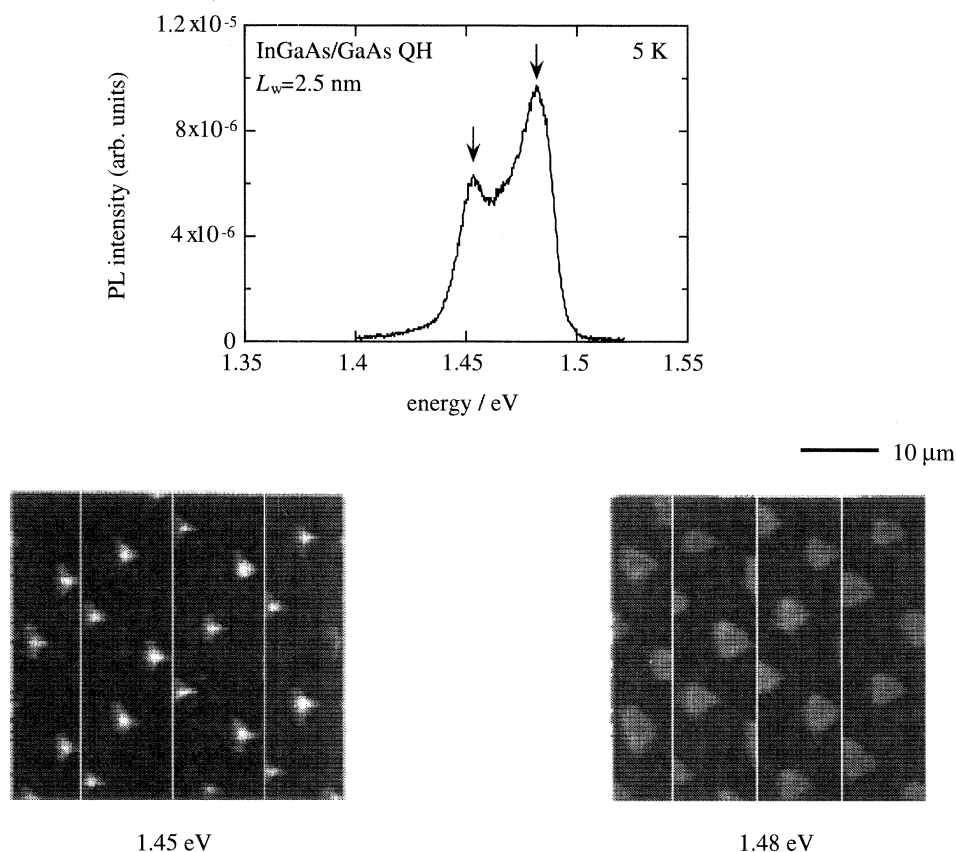1.45 eV   1.48 eV

Figure 12. Photoluminescence spectrum and cathode-luminescence images obtained for InGaAs layer grown in the TSRs.

The image on the right corresponds to the higher energy peak and the image on the left corresponds to the lower energy peak. These two images have a complementary relationship. The image on the right shows a bright image at the side walls of the (111)A facet. The left image shows a clear bright image at the bottom of the TSR structure.

Magneto-PL at 4.2 K with the 5 nm thick InGaAs pseudomorphic heterostructure was measured with the magnetic field applied perpendicularly to the substrate. As the magnetic field increases, the higher energy peak increases by 11 meV, while the lower energy peak increases by 2 meV for 11.5 T. These results indicate the lateral confinement at the bottom of the TSR (Nagamune *et al.* 1992).

We would like to use this technology to investigate the physics of low-dimensional resonant tunnelling structures and to make quantum box emitters in RHET devices.

(c) *Self-assembled InAs dot and possible tunnelling devices*

Recently, there has been a lot of research into self-assembled InAs dots, mainly because of their potential for use in the development of quantum-box lasers on GaAs substrates with low threshold current. This is because the sharp state density of quantum box is expected to improve laser performance by using them as the active
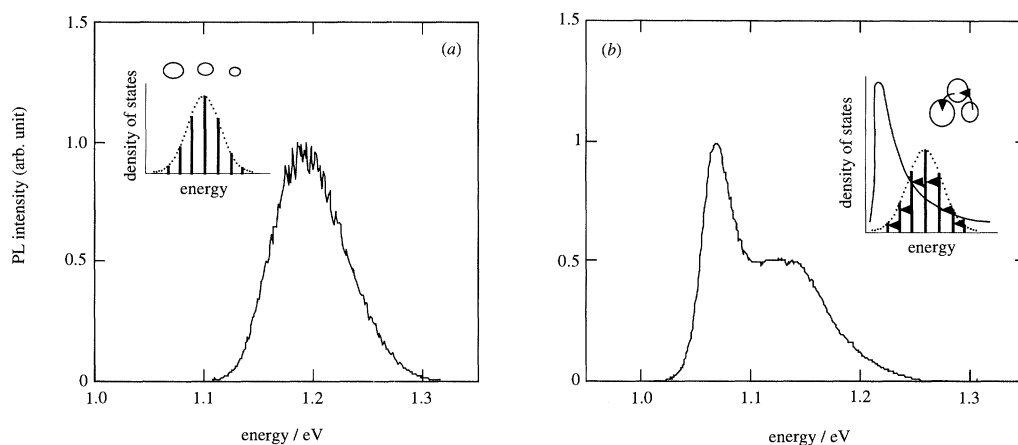
Figure 13. PL spectra of conventional quantum dots and multi-coupled quantum dots. (*a*) Conventional quantum dots. (*b*) Multi-coupled quantum dots.

layer of a semiconductor laser (Arakawa *et al.* 1982). However, there is still the problem of size fluctuation during fabrication. The size fluctuation distributes the state density over a wide energy range, resulting in spectrally broad luminescence. This broadening spoils the sharp state density of quantum dot arrays. This section describes a method to narrower and stronger photoluminescence from quantum dots using cascade-like carrier tunnelling among quantum dots (Tackeuchi *et al.* 1995).

The InAs layers were grown at a rate of 90 nm per hour to a coverage of 2.5 monolayers at an As pressure of 6×10^{-6} Torr by MBE. Quantum dots have a mean base diameters of 26 nm with a standard deviation of 11%. The average distance to the nearest neighbour in the dots is 26 nm from centre to centre. This short distance means that the base of a quantum dot makes contact with the base of one adjacent quantum dot.

Thus the carriers in quantum dots seem to have a sufficient probability of tunnelling to the adjacent quantum dots. We call these multi-coupled quantum dots. When we grow quantum dots with an InAs deposition of 1.8 ML, the average distance between quantum dots is 43 nm, larger than the diameter of quantum dots. This indicates that quantum dots are isolated from each other. We call these conventional InAs dots.

Figure 13 shows the CW PL spectra of conventional quantum dots and multi-coupled quantum dots. The conventional quantum dots have a single and symmetrical peak. This symmetry can be ascribed to the distribution of the state density originated from the size fluctuation. On the other hand, the PL of the high density quantum dots shown on the right of the figure has two peaks. Since a wavefunction of carriers in a quantum dot penetrates into the adjacent dots, photoexcited carriers tunnel and relax into the quantum levels in the larger and energetically-lower quantum dots. Then the carriers finally reach the energetic load minimum and radiate. This process is expected to reduce the spectral width of PL below that of the original distribution of the state density, and also to enhance the peak PL intensity. The sharp peak at 1.07 eV is ascribed to the luminescence from these local minima, although the high energy peak at 1.14 eV is attributed to the distribution of the state density. Clearly, the intensity of the low-energy peak is twice that of the high-energy peak, and the width of the low energy peak becomes narrower than half the high energy
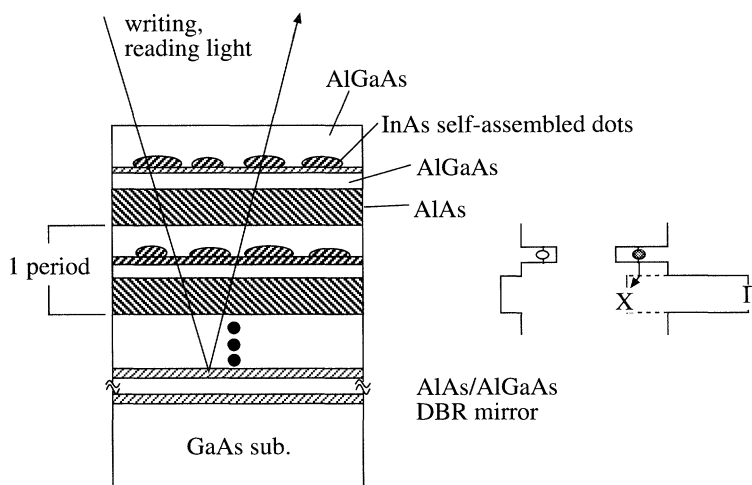
N. Yokoyama and others

Figure 14. InAs quantum dot hole-burning memory device.

peak. At room temperature, the PL wavelength shifts to 1.24 mm. This near-1.3 mm wavelength is very useful for optical-fibre based communication systems.

Figure 14 shows one possible InAs quantum dot hole-burning memory device. The device consists of an AlAs/AlGaAs DBR mirror, periodically stacked AlAs layers, and InAs dots embedded in AlGaAs layers. A writing and reading laser beam is shone from the surface and reflected by the DBR mirror. By shining the writing beam at a particular wavelength, electron-hole pairs are created in the InAs dots, which have the same absorption energy as the photon energy. When two holes with both spin-directions are created in the ground state of a quantum box, its ground level absorption is perfectly bleached. In this device structure, electrons can tunnel out to the X-minimum of the AlAs layer, while holes remain in the InAs dots. This indicates that we can use this as a hole-burning material.

Thus there will be various applications in areas where tunnelling in quantum box structures is used.

6. Summary

In summary, logic and memory circuits could be constructed with fewer transistors and resistors using multi-emitter RHETs. Based on this technology, our research on this quantum functional device will continue in three different directions.

One is to develop quantum functional devices further, and to integrate these devices with complementary-HEMT logic circuits in next-century cryoelectronic systems. New architectures such as non von-Neumann memory-based architecture might be used in particular cases. The second direction is to develop room temperature quantum functional bipolar devices which will possibly replace GaAs HBTs. The third direction is to develop quantum box devices, aiming at terabit-memory devices. This technology will also be useful in the development of photonic devices such as quantum dot lasers and new photonic memory devices.

References

Arakawa, Y. & Sakaki, H. 1982 Multidimensional quantum well laser and temperature dependence of its threshold current. *Appl. Phys. Lett.* **40**, 939–941.

Imamura, K., Takatsu, M., Mori, T., Muto, S. & Yokoyama, N. 1994 Open-base multi-emitter HBTs with increased logic functions. In *Extended Abstracts of the 1994 Int. Conf. on Solid State Devices and Materials*, pp. 467–469.

Mori, T., Muto, S., Tamura, H. & Yokoyama, N. 1993 An SRAM cell using a double-emitter RHET for gigabit-plus memory applications. In *Extended Abstracts of the 1993 Int. Conf. Solid-State Devices and Materials*, pp. 1074–1076.

Nagamune, Y., Arakawa, Y., Tsukamoto, S. & Nishioka, M. 1992 Photoluminescence spectra and anisotropic energy shift of GaAs quantum wires in high magnetic fields. *Phys. Rev. Lett.* **69**, 2963–2966.

Sakuma, Y., Sugiyama, Y., Muto, S. & Yokoyama, H. 1994 New approach to AlAs/GaAs quantum dot structures using MOVPE on tetrahedral-shaped recesses formed on (111)B GaAs substrates. *21st Int. Symp. on Compound Semiconductors*, San Diego.

Tackeuchi, A., Nakata, Y., Muto, S., Inata, T., Usuki, T., Sugiyama,Y., Yokoyama, N. & Wada, O. 1995 InAs/GaAs multi-coupled quantum dots structure enabling high-intensity, near-1.3-mm emission due to cascade carrier tunneling. In *Int. Conf. on Solid State Devices and Materials*, Osaka, pp. 719–721.

Takatsu, M., Imanura, K., Mori, T., Adachihara, T., Muto, S. & Yokoyama, N. 1994 Logic circuits using multi-emitter resonant-tunneling hot electron transistors (RHETs). Paper No. TA 7.2 reported at ISSCC.

Yokoyama, N., Imamura, K., Muto, S., Hiyamizu, S. & Nishi, H. 1985 A new functional resonant-tunneling hot electron transistor (RHET). *Jpn. J. Appl. Phys.* **24** L853–854.
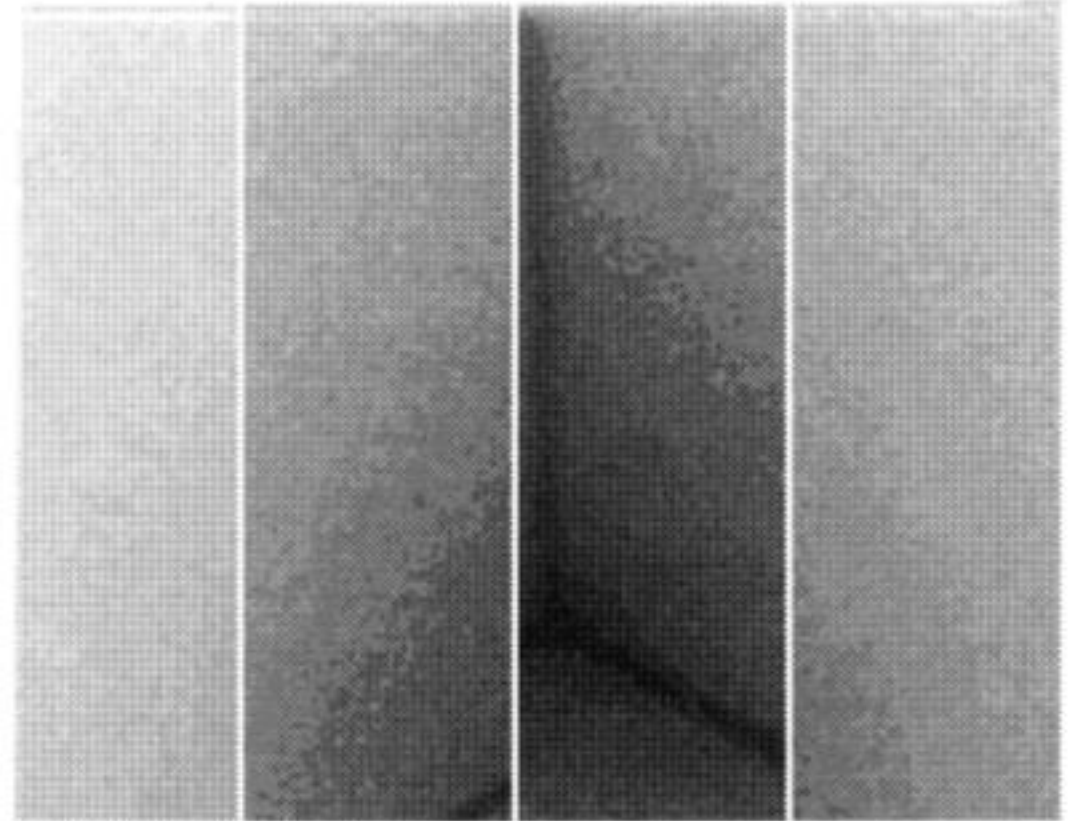
SiO₂
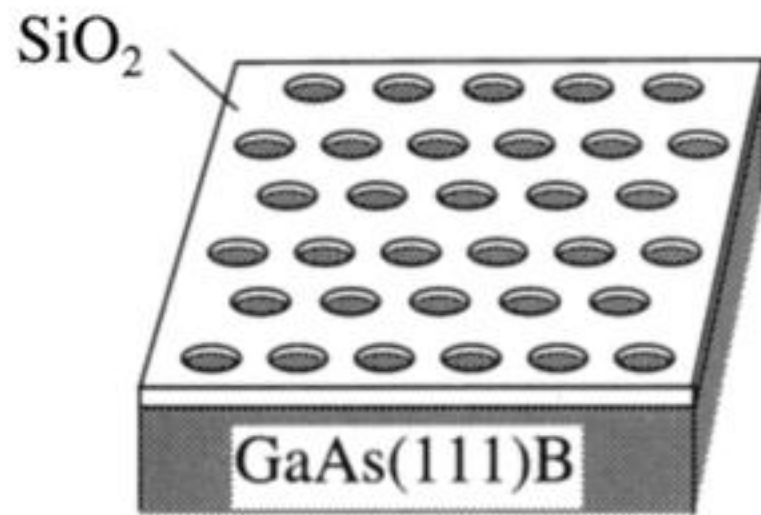
GaAs(111)B

1. Use of GaAs (111)B substrates

2. Anisotropic etching

Etchant: 1% Br_2-ethanol solution
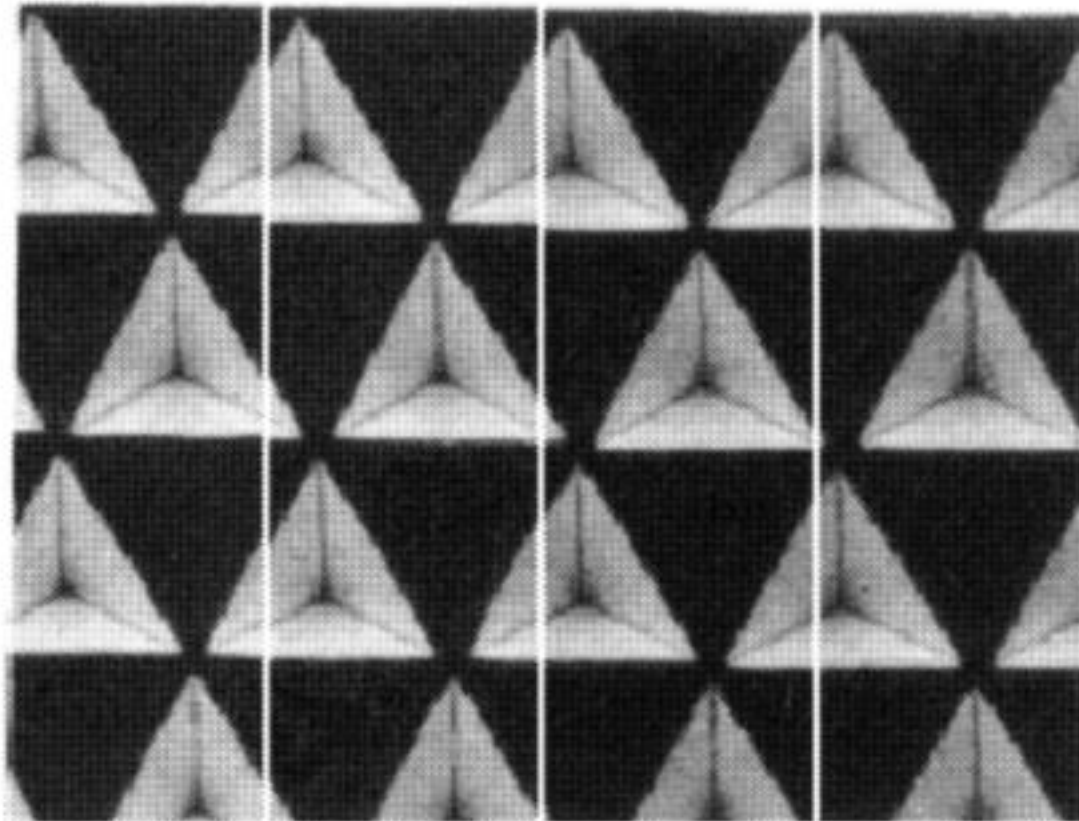
4 μm

200 nm

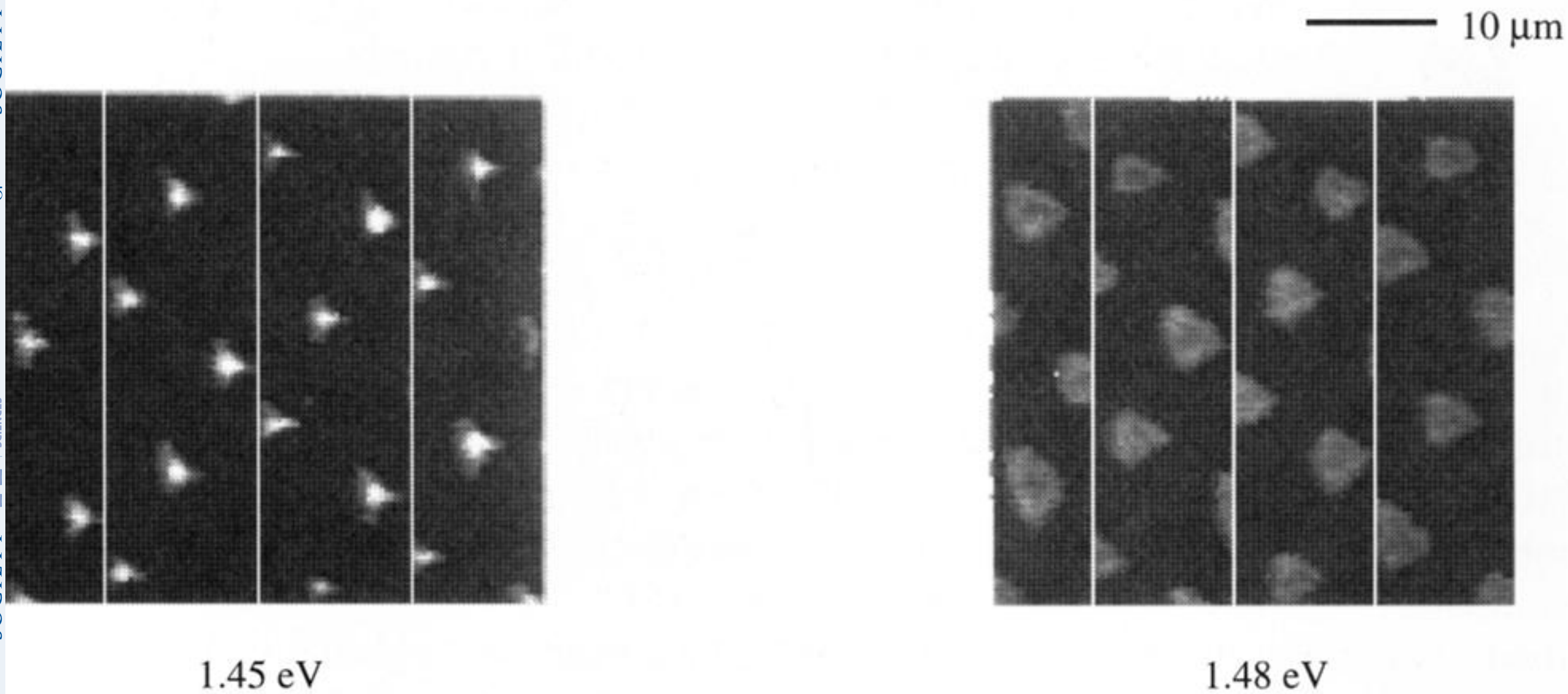Figure 11. Inverted tetrahedral-shaped recesses (TSR) using GaAs (111)B substrates.
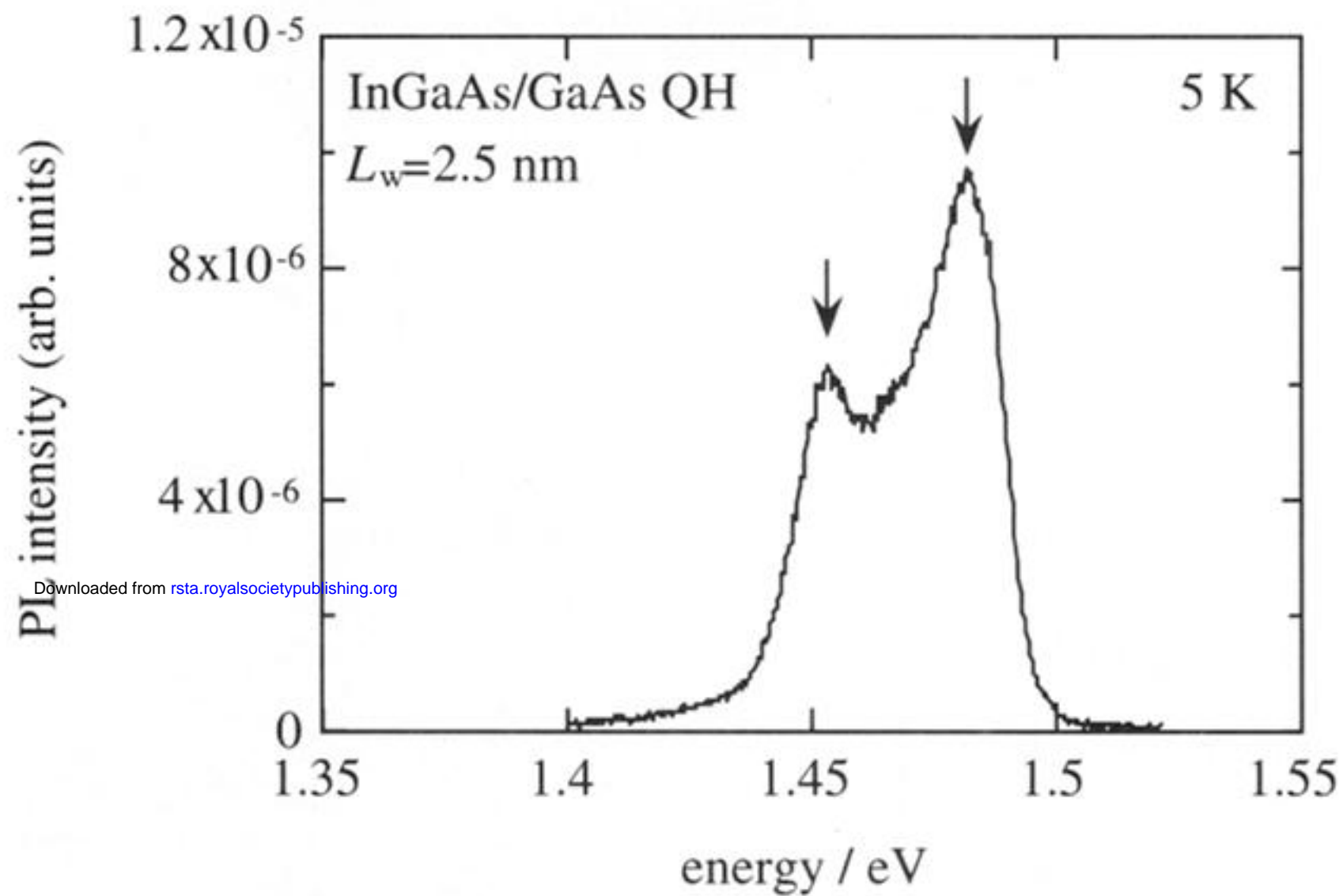
Figure 12. Photoluminescence spectrum and cathode-luminescence images obtained for InGaAs layer grown in the TSRs.